WE CLAIM:

1. A memory device comprising a plurality of magneto-resistive bits, the memory device comprising:

a first bit end at one end of each of the magneto-resistive bits;

a first contact structure contacting the first bit end, wherein the first bit end is dimensioned to extend around the first contact structure;

a second bit end at an other end of each of the magneto-resistive bits;

a second contact structure contacting the second bit end, wherein the second bit end is dimensioned to extend around the second contact structure; and

a central section elongated along a length between the first bit end and the second bit end of each of the magneto-resistive bits.

2. The memory device of Claim 1, wherein a width of the first bit end is greater than a width of the central section.

3. The memory device of Claim 2, wherein a width of the second bit end is greater than the width of the central section.

4. An integrated circuit comprising a magneto-resistive bit, the integrated circuit comprising:

a first bit end at one end of the magneto-resistive bit; and

a first contact structure contacting the first bit end,

wherein the first bit end is dimensioned to extend around the first contact structure, wherein the magneto-resistive bit further comprises an elongate central section having a width and extending along a length from the first bit end, the first bit end having a width that is greater than the width of the elongate central section.

5. The integrated circuit of Claim 4, further comprising:

an insulating layer positioned adjacent the magneto-resistive bit, the insulating layer defining a first hole having a perimeter, wherein the first hole extends through the insulating layer to the first bit end, the first bit end having a perimeter and being dimensioned such that the perimeter of the first bit end extends laterally beyond the perimeter of the first hole.

6. The integrated circuit of Claim 5, wherein the insulating layer comprises silicon nitride.

7. The integrated circuit of Claim 5, wherein the first contact structure comprises a metallic material that extends down through the first hole and electrically contacts the first bit end.

8. The integrated circuit of Claim 7, wherein the metallic material comprises aluminum.

9. The integrated circuit of Claim 7, wherein the metallic material comprises copper.

10. The integrated circuit of Claim 7, wherein the metallic material comprises a titanium tungsten plug.

11. The integrated circuit of Claim 5, further comprising a protective layer interposed between the first bit end and the insulating layer at least in the region of the first hole.

12. The integrated circuit of Claim 11, wherein the protective layer is at least partially conductive.

13. The integrated circuit of Claim 11, wherein the protective layer is an etch stop layer.

14. The integrated circuit of Claim 13, wherein the first hole is formed using a selective chemical etch that stops at the etch stop layer.

15. The integrated circuit of Claim 11, wherein the protective layer comprises chrome-silicon.

16. The integrated circuit of Claim 4, further comprising:

a second bit end at an other end of the elongate central section, wherein a second contact structure contacts the second bit end.

17. The integrated circuit of Claim 16, wherein the second bit end is dimensioned to extend around the second contact structure.

18. The integrated circuit of Claim 16, wherein the second bit end has a width that is greater than the width of the elongate central section.

19. An integrated circuit comprising a magneto-resistive bit, the integrated circuit comprising:

the magneto-resistive bit having an elongated central section having a width;

the magneto-resistive bit having a first bit end at one end of a length of the elongated central section, the first bit end having a width that is greater than the width of the elongated central section;

the magneto-resistive bit having a second bit end at the other end of the length of the elongated central section, the second bit end having a width that is greater than the width of the elongated central section;

a first contact structure for providing an electrical contact to the first bit end, the first contact structure having a first contact structure perimeter at an interface with the first bit end; and

a second contact structure for providing an electrical contact to the second bit end, the first contact structure having a second contact structure perimeter at an interface with the first bit end,

wherein the first bit end is dimensioned to extend around the first contact structure perimeter and wherein the second bit end is dimensioned to extend around the second contact structure perimeter.

20. The integrated circuit of Claim 19, further comprising an insulating layer positioned adjacent the magneto-resistive bit, the insulating layer defining a first hole accommodating the first contact structure, wherein the first hole extends through the insulating layer to the first bit end.

21. The integrated circuit of Claim 20, further comprising an insulating layer positioned adjacent the magneto-resistive bit, the insulating layer defining a second hole accommodating the second contact structure, wherein the second hole extends through the insulating layer to the second bit end.